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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/977,301	10/16/2001	Teruyoshi Kawai	110885	4683

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OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
TRIMMINGS, JOHN P	
ART UNIT	**PAPER NUMBER**
2133	3

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/977,301	KAWAI, TERUYOSHI	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-16 are presented for examination.

Priority

The examiner acknowledges the priority date of 10/24/2000 based on 35 USC 119.

Drawings

1. Figure 8 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an

> international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 1 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Organ et al., U.S. Patent No. 6449741.

As per Claim 1:

Organ et al. teaches an analog/digital characteristics testing device (column 1 lines 34-37) comprising: a plurality of measurement circuits for measuring an analog/digital characteristic of one or more ICs to be tested (FIG.4 62) in accordance with a test condition data (FIG.4 140); and a setting unit for setting a different test condition data to each measurement circuit (FIG.4 108).

As per Claim 9:

Organ et al. teaches an IC testing apparatus (column 1 lines 10-13) comprising: an analog/digital characteristics testing device (column 1 lines 34-37) comprising: a plurality of measurement circuits for measuring an analog/digital characteristic of one or more ICs to be tested (FIG.4 62) in accordance with a test condition data (FIG.4 140); and a setting unit for setting a different test condition data to each measurement circuit (FIG.4 108).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 2, 4-5, 10, and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Organ et al., U.S. Patent No. 6449741 as applied to Claim 1 or 9 above, and in view of Shigeru Sugamori, U.S. Patent No. 6536006.

As per Claim 2:

The analog/digital characteristics testing device as claimed in claim 1 is further limited wherein the setting unit comprises a counting circuit that determines which measurement circuit is being addressed. Although Organ et al. does not teach a counter, an analogous art, Sugamori does. The referenced art teaches a test condition outputting circuit for outputting the test condition data in order (FIG.4 Test Controller 41); a counting circuit for counting the number of the test condition data outputted from the test condition outputting circuit (column 8 lines 61-67); and a specifying circuit for specifying the measurement circuit in which the test condition data is written (FIG.4 Interface 53), in accordance with a counter value of the counting circuit (column 8 lines 39-49). And Sugamori, in column 4 lines 64-67 and column 5 lines 1-4, boasts of the advantages of using the invention with an event-based memory within the measurement unit. And so,

one with ordinary skill in the art at the time of the invention, motivated as suggested by Sugamori, would combine the arts, thus the claim is rejected.

As per Claims 4 and 12:

The analog/digital characteristics testing device as claimed in claim 1 or 9 is limited to be further comprising a management unit for managing a test result data obtained by each measurement circuit. Sugamori, in FIG.4 66, 67 & 68, teaches such a circuit. And in view of the motivation previously stated, one with ordinary skill in the art at the time of the invention would combine the references, and so the claims are rejected.

As per Claims 5 and 13:

The analog/digital characteristics testing device as claimed in claim 4 or 12 is limited wherein the setting unit (Sugamori FIG.4 Tester Controller 41) comprises: a test condition outputting circuit for outputting the test condition data in order; and a counting circuit for counting the number of the test condition data outputted from the test condition outputting circuit (column 8 lines 61-67); and the management unit (FIG.4 66, 67 & 68) comprises: a multiplexing circuit for outputting the test result data obtained by each measurement circuit (FIG.4 67 and column 8 lines 50-60), from a predetermined output terminal in accordance with a counter value of the counting circuit (FIG.4 67 and column 8 lines 50-60); and a judging circuit for judging whether the one or more ICs to be tested are good or poor in accordance with the test result data outputted from the multiplexing circuit (FIG.4 Capture Memory 57). And in view of the motivation

previously stated, one with ordinary skill in the art at the time of the invention would combine the art, and therefore the claims are rejected.

As per Claim 10:

The IC testing apparatus as claimed in claim 9 is limited further, wherein the setting unit (Sugamori FIG.4 Tester Controller 41) comprises: a test condition outputting circuit for outputting the test condition data in order; a counting circuit for counting the number of the test condition data outputted from the test condition outputting circuit (column 8 lines 61-67); and a specifying circuit for specifying the measurement circuit in which the test condition data is written (FIG.4 Interface 53), in accordance with a counter value of the counting circuit (column 8 lines 50-60). And in view of the motivation previously stated, one with ordinary skill in the art at the time of the invention would combine the art, and therefore the claim is rejected.

6. Claims 3 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Organ et al., U.S. Patent No. 6449741, in view of Shigeru Sugamori, U.S. Patent No. 6536006 as applied to Claim 2 and 10 above, and further in view of the applicant's admitted prior art. The analog/digital characteristics testing device as claimed in claim 2 and 10 is limited wherein when an initial test condition data is outputted from the test condition outputting circuit, the specifying circuit specifies all of the measurement circuits as a circuit in which the initial test condition data is written. This is not taught in the references of Claim 2 or 10. However, the applicant, in FIG.8, and in pages 2 and 4 of the disclosure, discloses these attributes as pertaining to the prior art. One

with ordinary skill in the art at the time of the invention, motivated as already stated in Claim 2 and 10 above, would have found it to be obvious to combine the teachings so described, and so the claims are rejected.

7. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Organ et al., U.S. Patent No. 6449741, and further in view of the applicant's admitted prior art. Organ et al. teaches an analog/digital characteristics testing device (column 1 lines 34-37) comprising: a test condition output circuit for outputting test condition data (FIG.4 Tester Controller 90); a plurality of measurement circuits for measuring an analog/digital characteristic of one or more ICs to be tested (FIG.4 62) in accordance with a test condition data (FIG.4 140); and a setting unit for setting a different test condition data to each measurement circuit (FIG.4 108). However the reference fails to teach when an initial test condition data is outputted from the test condition outputting circuit, the specifying circuit specifies all of the measurement circuits as a circuit in which the initial test condition data is written. The applicant, in FIG.8, and in pages 2 and 4 of the disclosure, discloses these attributes as pertaining to the prior art. One with ordinary skill in the art at the time of the invention, motivated by Organ et al. to apply one tester to analog and digital testing (column 2 lines 55-67), would have found it to be obvious to combine the teachings so described, and so the claims are rejected.

8. Claims 7, 8, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Organ et al., U.S. Patent No. 6449741, and further in view of

the applicant's admitted prior art as applied to Claim 6 above, and further in view of Shigeru Sugamori, U.S. Patent No. 6536006.

As per Claims 7 and 15:

The analog/digital characteristics testing device as claimed in claim 6 or 14 is limited, wherein the setting unit comprises a counting circuit for counting the number of the test condition data outputted from the test condition outputting circuit (Sugamori column 8 lines 61-67); wherein the setting unit sets the test condition data to each measurement circuit in accordance with the number of test condition data (Sugamori FIG. 4 41), which is counted by the counting circuit (Sugamori column 8 lines 39-49). And in view of the motivation previously stated, one with ordinary skill in the art at the time of the invention would combine the teachings above, and so the claims are rejected.

As per Claims 8 and 16:

The analog/digital characteristics testing device as claimed in claim 6 or 14 is limited further comprising a multiplexing circuit for multiplexing a plurality of test result data obtained by measuring the analog/digital characteristic of the one or more ICs to be tested (FIG.4 Capture Memory 57) with the plurality of measurement circuits (FIG.4 67 and column 8 lines 50-60). And in view of the motivation previously stated, one with ordinary skill in the art at the time of the invention would combine the teachings above, and so the claims are rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on weekdays, 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

jpt

Albert DeCady
Primary Examiner